CLAIMS

1. A system comprising:

a first circuit;

a second circuit;

a serial communication link coupled to the first and second circuit;

a first interface coupled to the first circuit to transmit a data cell of n bits in response to a first in first out protocol; and

a second interface coupled to the second circuit to receive the data cell in response to the first in first out protocol.

2. The system of claim 1 wherein the first interface to transmit the data cell comprises a first converter to divide the data cell of n bits into smaller cells of less than n bits.

3. The system of claim 1 wherein the second interface to receive the data cell comprises a second converter to combine the data cells of less than n bits to generate a data cell of n bits.

4. The system of claim 1 wherein the first interface to transmit the data cell adds a plurality of error correcting bits to the data cell.

5. The system of claim 1 wherein the second interface to receive the data cell extracts a plurality of error correcting bits from the data cell.

6. The system of claim 1 wherein the serial communications link comprises twenty serial channels capable of transmitting 625 million bits a second.

7. A method comprising:

receiving a data cell of n bits in a first integrated device;

receiving a plurality of control bits and error correcting code bits;

appending the plurality of control bits and error correcting code bits to the data cell;

converting the data cell of n bits to a plurality of data cells of less than n bits;

transmitting the plurality of data cells of less than n bits from the first integrated device in a serial format in response to a first in first out protocol; and

receiving the plurality of data cells of less than n bits in a second integrated device.

8. The method of claim 7 further comprising:

re-converting the plurality of data cells of less than n bits to the data cell of n bits.

9. The method of claim 7 wherein transmitting the data cell of the plurality of data cells of less than n bits comprises validating the serial format with a resync operation.

10. The method of claim 8 wherein re-converting the plurality of data cells of less than n bits to the data cell of n bits comprises aligning the data cells of less than n bits in response to the error correcting code bits.

11. The method of claim 8 wherein re-converting the plurality of data cells of less than n bits to the data cell of n bits comprises extracting the control bits from the data cell of n bits

12. A system comprising:

a first network switch comprises a first transmit interface and a first receive interface ;

a second network switch comprises a second transmit interface and a second receive interface;

a data cell of n bits; and

a serial communication link coupled to the first and second network switch, to transmit the data cell from the first transmit interface of the first network switch to the second receive interface of the second network switch via a m bit by m bit crossbar buffer in response to a first in first out protocol.

13. The system of claim 12 wherein the first and second transmit interface comprise a converter to divide the data cell into a plurality of data cells of less than n bits.

14. The system of claim 12 wherein the first and second transmit interface generate and append a plurality of control and error correcting code bits to the data cell.

15. The system of claim 12 wherein the first and second transmit interface comprise a low voltage differential signaling encoder.

16. The system of claim 12 wherein the first and second receive interface comprise a low voltage differential signaling decoder.

17. The system of claim 12 wherein the first and second receive interface comprise a re-converter to align a plurality of data cells of less than n bits data cell into the data cell of n bits.